What is claimed is:

1. An integrated circuit device on a substrate, comprising:

a number of semiconductor surface structures spaced apart along the substrate;

a number of plugs contacting the substrate between the number of surface structures, wherein the number of plugs includes an inner plug and a pair of outer plugs, wherein the inner and the pair of outer plugs are formed by the method of:

forming a first opening in a first isolation layer on the semiconductor surface structures, wherein forming the first opening includes exposing portions of the multiple semiconductor surface structures, and includes exposing portions of the substrate between the multiple surface structures;

depositing a first conductive material in the first opening to cover the multiple surface structures;

forming a second isolation layer across the first conductive material;

etching the first conductive material and the second isolation layer to form a second opening in the first conductive material in a source region on the substrate, wherein the second opening exposes portions of an adjacent pair of the multiple surface structures;

forming spacers on interior walls of the second opening, wherein forming the spacers includes separating the first conductive material into the inner plug and the pair of outer plug, wherein the inner plug is isolated beneath and between the adjacent pair, wherein the outer plugs cover part of top portions of the adjacent pair; and

forming a second conductive material in the second opening, whereby the second conductive material contacts the inner plug and is isolated from the outer plugs by the spacers.

2. A memory device, comprising:

multiple insulated wordlines having top surfaces, wherein the insulated wordlines are spaced apart from one another and formed on a substrate;

a bitline plug located between an adjacent pair of the insulated wordlines, the bitline plug having a top surface beneath the top surfaces of the insulated wordlines;

a pair of storage node plugs located on the opposite side of the adjacent pair of insulated wordlines from the bitline plug,

a bitline coupled to the bitline plug, wherein the bitline, the bitline plug, and the storage node are formed by the method of:

depositing a conductive material over the multiple insulated wordlines on the substrate;

etching a portion of the conductive material over a pair of insulated wordlines to form the bitline plug and the pair of storage node plugs, wherein the bitline plug is in between and beneath the pair of insulated wordlines and separated from the storage node plugs, wherein top portion of each of the storage node plugs covers a part of top surface of one insulated wordlines of the pair of insulated wordlines;

forming a pair of opposing spacers between the bitline plug and the pair of storage node plugs; and

forming the bitline over the bitline plug, wherein the bitline is separated from the storage node plugs by the pair of opposing spacers.

3. A data handling system, comprising:

a central processing unit;

a memory device, wherein the memory device comprises:

multiple insulated wordlines having top surfaces, wherein the insulated wordlines are spaced apart from one another and formed on a substrate;

a bitline plug located between an adjacent pair of the insulated wordlines, the bitline plug having a top surface beneath the top surfaces of the insulated wordlines;

a pair of storage node plugs located on the opposite side of the adjacent pair of insulated wordlines from the bitline plug,

a bitline coupled to the bitline plug, wherein the bitline, the bitline plug, and the storage node are formed by the method of:

depositing a conductive material over the multiple insulated wordlines on the substrate;

etching a portion of the conductive material over a pair of insulated wordlines to form the bitline plug and the pair of storage node plugs, wherein the bitline plug is in between and beneath the pair of insulated wordlines and separated from the storage node plugs, wherein top portion of each of the storage node plugs covers a part of top surface of one insulated wordlines of the pair of insulated wordlines;

forming a pair of opposing spacers between the bitline plug and the pair of storage node plugs; and

forming the bitline over the bitline plug, wherein the bitline is separated from the storage node plugs by the pair of opposing spacers.